

LESSION PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	6.1.14	Introduction to AP 8085	I	CR		
2	7.1.14	Introduction to 8086 Architecture	I	"		
3	7.1.14	Register organization & signal description of 8086	I	"		
4	10.1.14	Physical memory organization & addressing capability	I			
5	11.1.14	Minimum mode & maximum mode of 8086	I			
6	17.1.14	Addressing modes of 8086	I			
7	18.1.14	Instruction set of 8086	I	"		
8	20.1.14	Assembler directives & operators	I	"		
9	21.1.14	Machine level programming	I	CR		
10	23.1.14	Stack structure of 8086	II	"		
11	24.1.14	Interrupts of 8086	II	"		
12	25.1.14	Interrupt cycle of 8086	II			
13	27.1.14	Nonmaskable & maskable interrupts	II	"		
14	28.1.14	Interrupt programming	II			
15	30.1.14	Semiconductor memory interfacing	III	CR		
16	31.1.14	dynamic RAM interfacing	III	"		
17	1.2.14	Interfacing I/O ports	III	"		
18	3.2.14	P8255 PPI modes of operation of 8255	IV	"		
19	4.2.14	Interfacing D/A & A/D converters	IV	"		
20	6.2.14	Stepper motor interfacing	IV	"		

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Period	Date	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
21	7-2-14	Programmable Interrupt Controller 8259A	IV	CR		
22	10-2-14	Keyboard Controller 8279	IV			
23	11-2-14	8251 UART	IV			
24	12-2-14	DMA Controller 8257	IV			
25	14-2-14					
26	15-2-14	Programmable cilt	IV			
27	17-2-14	DMA Introd. 8257	IV			
28	18-2-14	Features of 80386 & architecture of 80386	V	CR		
29	20-2-14	Signal description of 80386	V			
30	21-2-14	Register organization of 80386	V			
31	22-2-14	Addressing modes of 80386	V			
32	24-2-14		V			
33	25-2-14	Data type of 80386	V			
34	1-3-14	protected mode of 80386	V			
35	3-3-14	Segmentation & paging	V			
36	4-3-14	Virtual & enhanced mode of 80386	V			
37	6-3-14	Instruction set of 80386	V			
38	7-3-14	The coprocessor 80387	V			
39	8-3-14	CPU with a numeric coprocessor 80486 DX	V			
40	10-3-14	Introduction to 8051 micro controller	VI	CR		

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41	11-3-14	8051 pin description	<u>VI</u>	CR		
42	12-3-14	I/O ports of 8051	<u>VI</u>	"		
43	14-3-14	Memory organization of 8051	<u>VI</u>	"		
44	15-3-14	MC 8051 Addressing modes	<u>VI</u>	"		
45	17-3-14	Assembly language programming	<u>VI</u>	"		
46	18-3-14	features of 8051	<u>VI</u>	"		
47	20-3-14	8051 I/O ports	<u>VI</u>	"		
48	21-3-14	features of 8051	<u>VI</u>	CR		
49	22-3-14	8051 I/O ports	<u>VI</u>	"		
50	24-3-14	8051 I/O ports	<u>VI</u>	"		
51	25-3-14	8051 I/O ports	<u>VI</u>	"		
52	27-3-14	8051 I/O ports	<u>VI</u>	"		
53	28-3-14	8051 I/O ports	<u>VI</u>	"		
54	29-3-14	8051 I/O ports	<u>VI</u>	"		
55	1-4-14	8051 I/O ports	<u>VI</u>	"		
56	2-4-14	8051 I/O ports	<u>VI</u>	CR		
57	4-4-14	8051 I/O ports	<u>VI</u>	"		
58	5-4-14	8051 I/O ports	<u>VI</u>	"		
59	7-4-14	8051 I/O ports	<u>VI</u>	"		
60	8-4-14	8051 I/O ports	<u>VI</u>	"		

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